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Mohamad Hammam Alsafrjalani and Ann Gordon-Ross . Dynamic Cache Tuning in Consumer-based Embedded Devices
Xiaotao Jia, Yici Cai, Qiang Zhou and Bei Yu. A Redundant Via Insertion Enhanced Concurrent Detailed Router
Hang Zhang, Xuhao Chen, Nong Xiao, Zhiguang Chen and Fang Liu. Red-Shield: Shielding Read Disturbance for STT-RAM Based Register files on GPUs
Hu Qingda, Sun Guangyu, Shu Jiwu and Zhang Chao. Exploring Main Memory Design based on Racetrack Memory Technology
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Tosiron Adegbija . Exploring Configurable Non-Volatile Memory-based Caches for Energy-Efficient Embedded Systems
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volatile Last Level Caches with Cluster Mapping

[Munish Jassi](#), Uzair Sharif, [Daniel Müller-Gritschneider](#) and [Ulf Schlichtmann](#). Hardware-Accelerated Software Libraries Drivers Generation for IP-Centric SoC Designs

Marcelo Ruaro and Fernando Gehm Moraes. Dynamic Real-Time Scheduler for Large-Scale MPSoCs

Naman Saraf and Kia Bazargan. Polynomial Arithmetic Using Sequential Stochastic Logic

Cosimo Aprile, Luca Baldassarre, Vipul Gupta, Juhwan Yoo, Mahsa Shoaran, Yusuf Leblebici and Volkan Cevher. Learning Based Near-Optimal Area-Power Trade-offs in Hardware Design for Neural Signals Acquisition

Yongsuk Choi and [Yong-Bin Kim](#). A Novel On-Chip Impedance Calibration Method for LPDDR4 Interface between DRAM and AP/SoC

Xijing Han, Marco Donato, Iris Bahar, Alexander Zaslavsky and William Patterson. Design of Error-Resilient Logic Gates with Reinforcement Using Implications

Aditya Dalakoti, Carrie Segal, Merritt Miller and Forrest Brewer. Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection

Keshab Parhi and Yin Liu. Computing Complex Functions using Factorization in Unipolar Stochastic Logic

Xiaolin Xu and Daniel Holcomb. A Clockless Sequential PUF with Autonomous Majority Voting

[Ameey Kulkarni](#), Tahmid Abtahi, Emily Smith and [Tinoosh Mohsenin](#). Low Energy Sketching Engines on Many-Core Platform for Big Data Acceleration

Divya Pathak, Mohammad Hajkazemi, Mohammad Tavana, Houman Homayoun and Ioannis Savidis. Load Balanced On-Chip Power Delivery for Average Current Demand

[Hassan Afzali-Kusha](#), [Alireza Shafaei](#) and [Massoud Pedram](#). Optimizing the Operating Voltage of Tunnel FET-Based SRAM Arrays Equipped with Read/Write Assist Circuitry

Pei Luo, Cheng Li and Yunsi Fei. Concurrent Error Detection for Reliable SHA-3 Design

Travis Boraten, Avinash Kodi and Dominic Ditomaso. Secure Model Checkers for Network-on-Chip (NoC) Architectures

Vincent Mirian and Paul Chow. Extracting Designs of Secure IPs using FPGA CAD Tools

Adam Page, Nasrin Attaran, Colin Shea, Houman Homayoun and Tinoosh Mohsenin. Low-Power ManyCore Accelerator for Personalized Biomedical Applications

Xueyan Wang, Qiang Zhou, Yici Cai, Jianlei Yang, Mingze Gao and Gang Qu. Secure and Low-Overhead Circuit Obfuscation Technique with Multiplexers

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Fabrizio Lombardi, Jie Han and Salin Junsangri. A Design of a Non-Volatile PMC-Based (Programmable Metallization Cell) Register File

Fabrizio Lombardi, Kazuteru Namba and Wei Wei. Design and Comparative Evaluation of a Hybrid Cache Memory at Architectural Level

Ravi Patel, Eby Friedman and Praveen Raghavan. Exploratory Power Noise Models of Standard Cell 14, 10, and 7 nm FinFET ICs

[Md Farhadur Reza](#), Dan Zhao and Hong-Yi Wu. Task-Resource Co-allocation For Hotspot Minimization in Many-core NoCs

Hamed Tabkhi, Majid Sabbagh and Gunar Schirner. Guiding Power/Quality Exploration for Communication-Intense Stream Processing
Nidhi Batra, Pawan Sehgal, Shashwat Kaushik, Mohammad S. Hashmi and Anuj Grover. Static Noise Margin based Yield Modelling of 6T SRAM for Area and Minimum Operating Voltage Improvement using Recovery Techniques
Subrata Das, Soma Das, Adrija Majumdar, Parthasarathi Dasgupta and Debesh Kumar Das. Delay estimates for Graphene nanoribbons: a novel measure of fidelity and experiments with global routing trees
Jordi Pérez-Puigdemont and Francesc Moll. ASIC implementation of an all-digital self-adaptive PVTA variation-aware clock generation system
Ning Liu, Caiwen Ding, Yanzhi Wang and Jingtong Hu. Neural Network-based Prediction Algorithms for In-Door Multi-Source Energy Harvesting System for Non-Volatile Processors
Adam Watkins and Spyros Tragoudas. An Enhanced Analytical Electrical Masking Model for Multiple Event Transients
Daniel Kumar and Hae-Seung Lee. A Sampling Clock Skew Correction Technique for Time-Interleaved SAR ADCs