

GLSVLSI 2007

Sunday, March 11th

Sunday Tutorial: Thermal Modeling and Thermal-Aware Design in Nanometer Technologies: 2:00pm – 6:00pm
Organized by Prof. Mircea Stan, University of Virginia, USA
GARDENIA ROOM (Ground Floor)

Monday, March 12th

Opening: 8:15am – 8:30am

Keynote Speech 1: 8:30am – 9:15am

Philippe Magarshack, STMicroelectronics, France

Design Challenges in 45nm and Below: DFM, Low-Power and Design for Reliability

GARDENIA ROOM (Ground Floor)

Session 1A: Architecture and Memory: 9:15am – 10:55am

Session Chair: Marcello Lajolo, NEC LABS, USA

MERIDIANA ROOM (1st Floor)

- 123 *(Best paper)* Improving Performance and Energy Consumption in Embedded Microprocessor Platforms with a Flexible Custom Coprocessor Data-path
Michalis Galanis and Costas goutis, University of patras, Patras, Greece
- 137 An Optimized Linear Skewing Interleave Scheme for On-chip Multi-access Memory Systems
Chunyu Liu, Xing Qin and Xiaolang Yan, Zhejiang University, Hangzhou, China
- 50 I-Cache Multi-Banking and Vertical Interleaving
Sangyeun Cho, University of Pittsburgh, Pittsburgh, USA
- 87 A VLSI Architecture Design of an Edge Based Fast Intra Prediction Mode Decision Algorithm for H.264/AVC
Shen Li, Xianghui Wei and Satoshi Goto, Waseda University, Kitakyushu City, Japan

Session 1B: Timing and Power Analysis: 9:15am – 10:55am

Session Chair: Prof. Massimo Poncino, Politecnico di Torino, Italy

GARDENIA ROOM (Ground Floor)

- 320 Nostra-XTalk : A predictive framework for accurate static timing analysis in UDSM VLSI circuits
Debasish Das, Ahmed Shebaita, Yehea Ismail, Hai Zhou and Kip Killpack, Northwestern University, Evanston, USA

- 201 Modeling and Estimating Leakage Current in Series-Parallel CMOS Networks
Paulo Butzen, Andre Reis, Chris Kim and Renato Ribas, UFRGS, Porto Alegre, Brazil
- 264 Probabilistic Gate-level Power Estimation using a Novel Waveform Set Method
Saeid Tahmasbi Oskuii, Per Gunnar Kjeldsberg and Einar J. Aas, Norwegian University of Science and Technology, Trondheim, Norway
- 155 Robust Wiring Networks for DfY Considering Timing Constraints
Philipp Panitz, Markus Olbrich, Juergen Koehl and Erich Barke, Institute of Microelectronic Systems, University of Hannover, Hannover, Germany

Session 1C: Test and Reliability: 9:15am – 10:55am

Session Chair: Prof. Alberto Macii, Politecnico di Torino, Italy

ORTENSIA ROOM (Basement Floor)

- 133 Simultaneous Reduction in Test Data Volume and Test Time for TRC- Reseeding
bin zhou, yizheng ye and yongsheng wang, Harbin Institute of Technology, Harbin, China
- 64 SEU Mitigation for SRAM-Based FPGAs through Dynamic Partial Reconfiguration
Cristiana Bolchini, Davide Quarta and Marco D. Santambrogio, Politecnico di Milano, Milano, Italy
- 249 Estimating Path Delay Distribution Considering Coupling Noise
Rajeshwary Tayade, Vijay Kiran Kalyanam, Sani Nassif, Michael Orshansky and Jacob Abraham, University of Texas at Austin, Austin, USA
- 165 Co-Evolutionary High-Level Test Synthesis
Soheil Aminzadeh and Saeed Safari, University of Tehran, Tehran, Iran

Coffee Break: 10:55am – 11:15am

**Session 2A: Device, Interconnect, and Power optimization for nano-CMOS:
11:15am – 12:55pm**

Session Chair: Azeez Bhavnagarwala, IBM, USA

MERIDIANA ROOM (1st Floor)

- 141 Optimizing FinFET Technology for High-Speed and Low-Power Design
Tarun Sairam, Wei Zhao and Yu (Kevin) Cao, Sun Microsystems Inc., Sunnyvale, USA
- 241 Analysis of Data Dependence of Leakage Current in CMOS Cryptographic Hardware
Jacopo Giorgetti, Giuseppe Scotti, Andrea Simonetti and Alessandro Trifiletti, University of Rome La Sapienza, Rome, Italy
- 9 Temperature-Aware Circuit Design Using Adaptive Body Biasing
Yan Zhang and Mircea Stan, University of Virginia, Charlottesville, USA
- 60 A Buffered Crossbar-Based Chip Interconnection Framework supporting Quality of Service
Ioannis Papaefstathiou, George Kornaros and Nikos Chrysos, Technical University of Crete, Chania, Greece

Session 2B: Emerging Technologies: 11:15am – 12:55pm

Session Chair: Prof. Mircea Stan, University of Virginia, USA

GARDENIA ROOM (Ground Floor)

- 222 Exact SAT-based Toffoli Network Synthesis
Daniel Grosse, Xiaobo Chen, Gerhard Dueck and Rolf Drechsler, University of Bremen, Bremen, Germany
- 142 Combinational Equivalence Checking for Threshold Logic Circuits
Tejaswi Gowda, Sarma Vrudhula and Goran Konjevod, Arizona State University, Tempe, USA
- 274 On-Chip Characterization of Molecular Electronic Devices using CMOS: The Design and Simulation of a Hybrid Circuit Based on Experimental Molecular Electronic Device Results
Nadine Gergel-Hackett, Garrett Rose, Peter Paliwoda, Christina Hacker and Curt Richter, National Institute of Standards and Technology, Gaithersburg, USA
- 301 Operation Limits in RTD-based Ternary Quantizers
Juan Núñez, José M. Quintana and María J. Avedillo, IMSE-CNM-CSIC, Sevilla, Spain

Session 2C: Low Power Architecture and Interconnect: 11:15am – 12:55pm

Session Chair: Prof. Massoud Pedram, University of Southern California, USA

ORTENSIA ROOM (Basement Floor)

- 226 Transition-activity Aware Design of Reduction-stages for Parallel Multipliers
Saeid Tahmasbi Oskui, Per Gunnar Kjeldsberg and Oscar Gustafsson, Norwegian University of Science and Technology, Trondheim, Norway
- 116 Reducing Snoop-Energy in Shared Bus-Based MPSoCs by Filtering Useless Broadcasts
Chun-Mok Chung and Jihong Kim, Seoul National Univ., Seoul, Korea
- 118 GALS SoC Interconnect Bus for Wireless Sensor Network Processor Platforms
Carlos Hernández, Rajkumar Raval and Chris Bleakley, University College Dublin, Dublin, Ireland
- 187 Sensitive Registers: a Technique for Reducing the Fetch Bandwidth in Low-Power Microprocessors
A Robinson and J Garside, The University of Manchester, Manchester, United Kingdom

Lunch and Poster Session 1: 12:55pm – 2:45pm

Poster Session 1:

CAMINO ROOM (Ground Floor)

- 4 Side-channel Resistant System level Design Flow for Public-key Cryptography
Kazuo Sakiyama, Elke De Mulder, Bart Preneel and Ingrid Verbauwhede, Katholieke Universiteit Leuven, Leuven-Heverlee, Belgium
- 25 Area Efficient Loop Filter Design for Charge Pump Phase Locked Loop
Raghavendra R G and Bharadwaj Amrutur, Indian Institute of Science, Bangalore, India
- 31 A New Approach to Logic Synthesis of Multi-Output Boolean Functions on PAL-based CPLDs
Dariusz Kania, Silesian University of Technology, Gliwice, Poland
- 42 A Novel Charge Recycler for TFT-LCD Source Driver IC
Dan Li, Tingcun Wei and Wei Wu, Northwestern Polytechnical University, Xi'an, China
- 56 Hardware-Efficient Propagate Partial SAD Architecture for Variable Block Size Motion Estimation in H.264/AVC
Zhenyu Liu, Yiqing Huang, Yang Song, Satoshi Goto and Takeshi Ikenaga, Kitakyushu Foundation, Kitakyushu, Japan

- 61 Compiler assisted architectural exploration for coarse grained reconfigurable arrays
Gregory Dimitroulakos, Nikos Kostaras, Michalis Galanis and Kostas Goutis, University Of Patras, Rio-Patras, Greece
- 73 Self-biased Charge Sampling Amplifier in 90nm CMOS for Medical Ultrasound Imaging
Linga Reddy Cenkeramaddi, Tajeshwar Singh and Trond Ytterdal, NTNU Trondheim, Trondheim, Norway
- 78 RT Level Reliability Enhancement by Constructing Dynamic TMRs
Naghmeh Karimi, Shahrzad Mirkhani, Zainalabedin Navabi and Fabrizio Lombardi, University of Tehran, Tehran, Iran
- 98 An Asynchronous FPGA Logic Cell Implementation
Atabak Mahram, Mehrdad Najibi and Hossein Pedram, Amirkabir University of Technology, Tehran, Iran
- 120 Real-time implementation of a time-frequency analysis scheme
Maurizio Martina, Andrea Molino, Fabrizio Vacca, Guido Masera, Andrea Terreno, Giorgio Pasquettaz and Giuseppe D'Angelo, Politecnico di Torino, Torino, Italy
- 124 Flexible blocks for high throughput Serially Concatenated Convolutional Codes
Maurizio Martina and Guido Masera, Politecnico di Torino, Torino, Italy
- 181 Novel Architectures for Efficient (m, n) Parallel Counters
Sreehari Veeramachaneni, Avinash Lingamneni, Kirthi Krishna Muntimadugu and Srinivas M.B, International Institute of Information Technology, Hyderabad, India
- 182 High CMRR Current Mode Operational Amplifier with a Novel Class AB Input Stage
Mustafa Altun and Hakan Kuntman, Istanbul Technical University, Istanbul, Turkey
- 185 Hardware architecture for matrix factorization in MIMO receivers
Barbara Cerato, Guido Masera and Peter Nilsson, Politecnico di Torino, Torino, Italy
- 200 Reduced-Complexity MIMO Detector with Close-to ML Error Rate Performance
Christian Hess, Markus Wenk, Andreas Burg, Christoph Studer, Peter Luethi, Norbert Felber and Wolfgang Fichtner, ETH Zurich, Zurich, Switzerland
- 204 Design and Realization of a Fault-Tolerant 90nm CMOS Cryptographic Engine Capable of Performing under Massive Defect Density
Milos Stanisavljevic, Frank Kagan Gürkaynak, Maria Gabrani, Alexandre Schmid and Yusuf Leblebici, Swiss Federal Institute of Technology EPFL, Lausanne, Switzerland
- 213 Exploring Subsets of Standard Cell Libraries to Exploit Natural Fault Masking Capabilities for Reliable Logic
Drew Ness, Christian J. Hescott and David J. Lilja, University of Minnesota Twin Cities, Minneapolis, USA
- 219 A Symmetric MOS Current-Mode Logic Universal Gate for High Speed Applications
Osman Abdulkarim and Maitham Shams, Carleton University, Ottawa, Canada
- 232 An Automated Unique Tagging System Using CMOS Process Variation
Brandon Dell, Jonathan Bolus and Travis Blalock, University of Virginia, School of Engineering and Applied Science, Charlottesville, USA
- 237 A Design Kit for a Fully Working Shared Memory Multiprocessor on FPGA
Antonino Tumeo, Matteo Monchiero, Gianluca Palermo, Fabrizio Ferrandi and Donatella Sciuto, Politecnico di Milano, Milan, Italy
- 260 Probabilistic Maximum Error Modeling for Unreliable Logic Circuits
Karthikeyan Lingasubramanian and Sanjukta Bhanja, University of South Florida, Tampa, USA
- 305 Critical Charge and SET Pulse Widths for Combinational Logic in Commercial 90nm CMOS Technology
Riaz Naseer, Jeff Draper, Younes Boulghasoul, Sandeepan DasGupta and Art Witulski, University of Southern California, Marina del Rey, USA

- 310 Active Bank Switching for Temperature Control of the Register File in a Microprocessor
Wonbok Lee, Kimish Patel and Massoud Pedram, USC, Los Angeles, USA

Keynote Speech 2: 2:45pm – 3:30pm

Massoud Pedram, University of Southern California, USA

Sleep Transistor Distribution in Row-Based MTCMOS Designs

Session Chair: Prof. Mircea Stan, University of Virginia

GARDENIA ROOM (Ground Floor)

Session 3A: Circuits and Logic: 3:30pm – 5:10pm

Session Chair: Prof. Giovanni De Micheli, EPFL, Switzerland

MERIDIANA ROOM (1stFloor)

- 191 A new decompression system for the configuration process of SRAM-based FPGAs
Luca Sterpone and Massimo Violante, Politecnico di Torino, Torino, Italy
- 321 Minimizing Peak Power in Synchronous Logic Circuits
Kambiz Rahimi, Impinj Inc., Seattle, USA
- 5 Linearized CMOS Active Resistor Independent on the Bulk Effect
Cosmin Popa, UPB, Buc, Romania
- 259 Structured and Tuned Array Generation (STAG) for High-Performance Random Logic
Matthew Ziegler, Gary Ditlow, Stephen Kosonocky, Zhenyu Qi and Mircea Stan, IBM T. J. Watson Research Center, Yorktown Heights, USA

Session 3B: Emerging Technologies for Low Power Design: 3:30pm – 5:10pm

Session Chair: Prof. Sanjukta Bhanja, University of South Florida, USA

GARDENIA ROOM (Ground Floor)

- 257 Design of Mixed Gates for Leakage Reduction
Frank Sill, Jiayi You and Dirk Timmermann, University of Rostock, Rostock, Germany
- 210 Dummy Fill Aware Buffer Insertion During Routing
Jia Yanming, Cai Yici and Hong Xianlong, Tsinghua University, Beijing, China
- 207 Analyzing and Modeling Process Balance for Sub-threshold Circuit Design
Joseph Ryan, Jiajing Wang and Ben Calhoun, University of Virginia, Charlottesville, USA
- 311 Viewing Direction-Aware Backlight Scaling
Chih-Nan Wu and Wei-Chung Cheng, National Chiao Tung University, Hsinchu, Taiwan

Session 3C: Digital Synthesis: 3:30pm – 5:10pm

Session Chair: Prof. Massimo Poncino, Politecnico di Torino, Italy

ORTENSIA ROOM (Basement Floor)

- 32 Synthesis of Irregular Combinational Functions with Large Don't Care Sets
Valentin Gherman, Hans-Joachim Wunderlich, Rio David Mascarenhas, Juergen Schloeffel and Michael Garbers, CEA-LIST, Saclay, France
- 308 DAG Based Library-Free Technology Mapping
Felipe Marques, Leomar Rosa Jr, Renato Ribas, Sachin Sapatnekar and Andre Reis, Nangate, Herlev, Denmark

- 186 Using Standard ASIC Back-End for QDI Asynchronous Circuits: Dealing with Isochronic Fork Constraint
Mehrdad Najibi, Kamran Saleh and Hossein Pedram, Amirkabir University of Technology, Tehran, Iran
- 251 An Evolutionary Approach for Standard-Cell Library Reduction
Andrea Ricci, Ilaria De Munari and Paolo Ciampolini, University of Parma, Parma, Italy

Coffee Break: 5:10pm – 5:30pm

Keynote Speech 3: 5:30pm – 6:15pm

Giovanni De Micheli, EPFL, Switzerland

Multi-Processor Operating System Emulation Framework with Thermal Feedback for Systems-on-Chip

GARDENIA ROOM (Ground Floor)

Dinner Banquet: 8:00pm – 10:30pm

Tuesday, March 13th

Keynote Speech 4: 8:30am – 9:15am

Sachin Sapatnekar, University of Minnesota

Computer-Aided Design of 3D Integrated Circuits

GARDENIA ROOM (Ground Floor)

Session 4A: Special Session - Embedded Tutorial: 9:15am – 10:55am

Jamil Kawa and Charles Chiang, Synopsys Inc., USA

DFM Issues for 65nm and Beyond

Session Chair: Prof. Yehia Massoud, Rice University, USA

MERIDIANA ROOM (1stFloor)

Session 4B: ASIP/ASIC: 9:15am – 10:55am

Session Chair: Prof. Philippe Coussy, Universite de Bretagne Sud, France

GARDENIA ROOM (Ground Floor)

- 268 Utilizing Custom Registers in Application-specific Instruction Set Processors for Register Spills Elimination
Hai Lin and Yunsi Fei, University of Connecticut, Storrs, USA
- 97 Implementation of a JPEG Object-Oriented ASIP A Case Study on a System-Level Design Methodology
Naser MohammadZadeh, Morteza NajafVand, Shaahin Hessabi and Maziar Goudarzi, Sharif university of technology, Tehran, Iran

- 188 Beyond 3G Wireless Communication System Prototype
Alberto Dassatti, Simone Zezza, Mario Nicola and Guido Masera, Politecnico di Torino, Torino, Italy
- 193 A new hardware architecture for performing the gridding of DNA microarray images
Luca Sterpone and Massimo Violante, Politecnico di Torino, Torino, Italy

Session 4C: System Level Design: 9:15am – 10:55am

Session Chair: Prof. Enrico Macii, Politecnico di Torino, Italy

ORTENSIA ROOM (Basement Floor)

- 221 A Design Methodology for Space-Time Adapter
CHAVET Cyrille, COUSSY Philippe, URARD Pascal and MARTIN Eric,
STMicroelectronics, Lorient, France
- 227 A Synchronization Algorithm for Local Temporal Refinements in Perfectly Synchronous Models with Nested Feedback Loops
Tarvo Raudvere, Ingo Sander and Axel Jantsch, KTH, Royal Institute of Technology, Stockholm, Sweden
- 119 HW/SW Partitioning using Discrete Particle Swarm
Amin Farmahini-Farahani, Mehdi Kamal and Sied Mehdi Fakhraie, School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran
- 69 Complexity-Constrained Partitioning of Sequential Programs for Efficient Behavioral Synthesis
Yuko Hara, Hiroyuki Tomiyama, Shinya Honda, Hiroaki Takada and Katsuya Ishii, Nagoya University, Nagoya, Japan

Coffee Break: 10:55am – 11:15am

Session 5A: CMOS & Logic Applications Optimization and Techniques:

11:15am – 12:55pm

Session Chair: Azeez Bhavnagarwala, IBM, USA

MERIDIANA ROOM (1stFloor)

- 131 Bus-encoding Technique to Reduce Delay, Power and Simultaneous Switching Noise (SSN) in RLC VLSI Interconnects
Raghunandan Chittarsu, Sainarayanan K S and Srinivas M B, International Institute of Information Technology (IIIT), HYDERABAD, India
- 34 A 5.4 GHz Wide Band Input and Output Matched Low Noise Amplifier
Roghoyeh Salmeh, University of Calgary, Calgary, Canada
- 114 A 900 MHz ISM Band MASH-12 Fractional-N Frequency Synthesizer for 5-Mbps Data Transmission.
Himanshu Arora, Nikolaus Klemmer and Patrick Wolf, Marvell Semiconductor, Santa Clara, USA
- 233 Design of an UHF RFID Transponder for Secure Authentication
Paolo Bernardi, Filippo Gandino, Bartolomeo Montrucchio, Maurizio Rebaudengo and Erwing Ricardo Sanchez, Politecnico di Torino, Torino, Italy

Session 5B: Verification Techniques: 11:15am – 12:55pm

Session Chair: Jamil Kawa, Synopsys Inc., USA

GARDENIA ROOM (Ground Floor)

- 160 Effective Heuristics for Counterexample-Guided Abstraction Refinement
Fei He, Xiaoyu Song, Ming Gu and Jiaguang Sun, Tsinghua University, Beijing, China
- 238 Reducing Verification Overhead with RTL slicing
Jen-Chieh Ou, Daniel G. Saab, Qiang Qiang and Jacob A. Abraham, CWRU, Cleveland, USA
- 174 Optimization Techniques for BDD-based Bisimulation Computation
Ralf Wimmer, Marc Herbstritt and Bernd Becker, Albert-Ludwigs-University Freiburg, Freiburg, Germany
- 176 Hardware-accelerated Path-Delay Fault Grading of Functional Test Programs for Processor-based Systems
Paolo Bernardi, Michelangelo Grosso and Matteo Sonza Reorda, Politecnico di Torino, Torino, Italy

Session 5C: Optimization and Verification: 11:15am – 12:55pm

Session Chair: Charles Chiang, Synopsys Inc., USA

ORTENSIA ROOM (Basement Floor)

- 109 An Approximation Algorithm for Fully Testable kEP-SOP Networks
Anna Bernasconi, Valentina Ciriani and Roberto Cordone, University of Milano, Crema (CR), Italy
- 298 A Coefficient Optimization and Architecture Selection Tool for SD Modulators Considering Component Non-Idealities
Orkun Saglamdemir, Omer Yetik, Selcuk Talay and Gunhan Dundar, Bogazici University, Istanbul, Turkey
- 121 Hand-in-hand Verification of High-level Synthesis
Chandan Karfa, Dipankar Sarkar and Chittaranjan Mandal, IIT Kharagpur, Kharagpur, India
- 208 Area Minimization Algorithm for Parallel Prefix Adders under Bitwise Delay Constraints
Taeko Matsunaga and Yusuke Matsunaga, FLEETS, Sawara-ku, Japan

Lunch and Poster Session 2: 12:55pm – 2:45pm

Poster Session 2:

CAMINO ROOM (Ground Floor)

- 28 A New Algorithm for the Largest Compositionally Progressive Solution of Synchronous Language Equations
Tiziano Villa, Svetlana Zharikova, Yevtushenko Nina, Brayton Robert and Sangiovanni-Vincentelli Alberto, University of Verona, Verona, Italy
- 36 An Efficient Cost Based Canonical Form for Boolean Matching
Giovanni Agosta, Francesco Bruschi and Donatella Sciuto, Politecnico di Milano, Milano, Italy
- 45 Substrate Noise Suppression Using Active Circuitry
Rashid Farivar, Simon Kristiansson, Fredrik Ingvarson and Kjell O. Jeppson, Department of Microtechnology and nanoscience, Chalmers university of technology, Göteborg, Sweden

- 76 The Effect of Temperature on Cache Size Tuning for Low Energy Embedded Systems
Hamid Noori, Maziar Goudarzi, Koji Inoue and Kazuaki Murakami, Kyushu University,
Fukuoka, Japan
- 82 Efficient Space-Time NoC Path Allocation based on Mutual Exclusion and Pre-reservation
Samuel EVAÏN and Jean-Philippe Diguët, UBS / CNRS, LORIENT, France
- 106 Skew Spreading For Peak Current Reduction
Zhengtao Yu, Marios Papaefthymiou and Xun Liu, NC State University, Raleigh, USA
- 108 Block Placement to Ensure Channel Routability
Shigetoshi Nakatake, Zohreh Karimi, Taraneh Taghavi and Majid Sarrafzadeh, University
of Kitakyushu, Kitakyushu, Japan
- 110 GA-SVM Feasibility Model and Optimization Kernel applied to Analog IC Design
Automation
Manuel Barros, IT-IST, Tomar, Portugal
- 171 Physical aware clock skew rescheduling
Xinjie Wei, Yici Cai and Xianlong Hong, Tsinghua University, Beijing, China
- 195 A Low-Power 333Mbps Mobile-Double Data Rate Output Driver with Adaptive Feedback
to minimize Overshoots and Undershoots
Rachit Kumar Gupta, Vikas Narang, Roopashree HM and Vinod Menezes, Texas
Instruments, India, Bangalore, India
- 202 Extended Register-Sharing in the Synthesis of Dual-Rail Two-Phase Asynchronous
Datapath
Koji Ohashi and Mineo Kaneko, Japan Advanced Institute of Science and Technology,
Nomi-shi, Japan
- 215 Three-Valued Specification and Verification of Analog Properties
Raffaella Gentilini, Klaus Schneider and Alexander Dreyer, University of Kaiserslautern,
Kaiserslautern, Germany
- 229 On the Energy Efficiency of Synchronization Primitives for Shared-Memory Single-Chip
Multiprocessors
Olga Golubeva, Mirko Loghi and Massimo Poncino, Politecnico di Torino, Torino, Italy
- 230 Improvements for Constraint Solving in the SystemC Verification Library
Daniel Grosse, Ruediger Ebendt and Rolf Drechsler, University of Bremen, Bremen,
Germany
- 231 Design of Cascode-Compensated Opamps Based on Settling Time and Open-Loop
Parameters
hamed aminzadeh and mohammad danaie, isl, masshad, Iran
- 235 DESIGN OF A FAMILY OF SLEEP TRANSISTOR CELLS FOR A CLUSTERED
POWER-GATING FLOW IN 65nm TECHNOLOGY
Andrea Calimera, Luca Benini, Alberto Macii, Enrico Macii, Massimo Poncino, Antonio
Pullini and Ashoka Visweswara Sathanur, Politecnico di Torino, Torino, Italy
- 236 StateCharts to SystemC: a High Level Hardware Simulation Approach
Marcello Mura, Marco Paolieri, Luca Negri and Maria Giovanna Sami, ALaRI, Lugano,
Switzerland
- 255 A Lightweight Parallel Java Execution Environment for Embedded Multiprocessor
Systems-on-Chip
Marco Mantovani, Simone Leardini, Martino Ruggiero, Andrea Acquaviva and Luca
Benini, University of Bologna, DEIS, Bologna, Italy
- 279 Improvement of power distribution network using correlation-based regression analysis
Shiho Hagiwara, Takumi Uezono, Takashi Sato and Kazuya Masu, Integrated Research
Institute, Tokyo Institute of Technology, Yokohama, Japan

- 280 A High-Level Register Optimization Technique for Minimizing Leakage and Dynamic Power
Deniz Dal and Nazanin Mansouri, Syracuse University, Syracuse, USA
- 294 An Efficient Net Ordering Algorithm for Buffer Insertion
Hamid Reza Kheirabadi and Morteza Saheb Zamani, Amirkabir University of Technology, tehran, Iran
- 306 An Efficient, End to End Fault Tolerant protocol for Networks on Chips
Muhammad Ali, Michael Welzl and Sven Hessler, University of Innsbruck, Innsbruck, Austria
- 316 Address Generation for Nanowire Decoders
Jia Wang, Hai Zhou and Ming-Yang Kao, Northwestern University, Evanston, USA

Keynote Speech 5: 2:45pm – 3:30pm

Kiyoo Itoh, Hitachi, Japan

Low-Voltage Limitations of Deep-Sub-100-nm CMOS LSIs —View of Memory Designers

GARDENIA ROOM (Ground Floor)

Session 6A: Arithmetic and Coding: 3:30pm – 5:10pm

Session Chair: Zhiyuan Yan, Lehigh University, USA

MERIDIANA ROOM (1stFloor)

- 105 Efficient pipelining for modular multiplication architectures in prime fields
Nele Mentens, Kazuo Sakiyama, Bart Preneel and Ingrid Verbauwhede, Katholieke Universiteit Leuven, Heverlee, Belgium
- 135 Design of a Versatile and Cost-Effective Hybrid Floating-Point/LNS Arithmetic Processor
Chichyang Chen and Paul Chow, Feng Chia University, Taichung, Taiwan
- 22 Multi-Segment GF(2^m) Multiplication and its Application to Elliptic Curve Cryptography
Jong-Soo OH and Dong-Ho LEE, Kyungpook National University, Daegu, Korea

Session 6B: Routing and Buffer Insertion: 3:30pm – 5:10pm

Session Chair: Hai Zhou, Northwestern University, USA

GARDENIA ROOM (Ground Floor)

- 38 Easy Floorplan Repair Using Dynamic Whitespace Management
Kristofer Vorwerk, Andrew Kennings, Doris Chen and Laleh Behjat, University of Waterloo, Kitchener, Canada
- 295 Improved Timing Closure by Early Buffer Planning in Floor-Placement Design Flow
Ali Jahanian and Morteza Saheb Zamani, Amirkabir University of Technology, Tehran, Iran
- 115 An Effective Buffer Planning Algorithm for IP Based Fixed-outline SOC Placement
Ou He, Sheqin Dong, Jinian Bian, Yuchun Ma and Xianlong Hong, Tsinghua University, Beijing, China
- 258 New Timing and Routability Driven Placement Algorithms for FPGA Synthesis
Yue Zhuo, Hao Li, Qiang Zhou and Yici Cai, University of North Texas, Denton, USA

Session 6C: Power Estimation and Modeling: 3:30pm – 5:10pm

Session Chair: Prof. Sanjukta Bhanja, University of South Florida, USA

ORTENSIA ROOM (Basement Floor)

- 71 RT-Level Vector Selection for Realistic Peak Power Simulation
Chia-Chien Weng, Ching-Shang Yang and Shi-Yu Huang, Electrical Engineering
Department, National Tsing-Hua University, HsinChu, Taiwan
- 92 A Fast Clock Scheduling for Peak Power Reduction in LSI
Yosuke TAKAHASHI, Yukihide KOHIRA and Atsushi TAKAHASHI, Tokyo Institute of
Technology, Meguro-ku Ookayama, Japan
- 216 A Path based Modeling Approach for Dynamic Power Estimation
Prashant Agrawal, Srinivasa R. STG, Ajit N. Oke and Saurabh Vijay, Indian Institute of
Technology Kharagpur, Kharagpur, India
- 153 Software Power Estimation using IPI(Inter-Prefetch Interval) Power Model for Advanced
Off-the-shelf Processor
Kyungsu Kang, Jungsoo Kim, Heejun Shim and Chong-Min Kyung, KAIST, DAEJEON,
Korea

Coffee Break: 5:10pm – 5:30pm

Keynote Speech 6: 5:30pm – 6:15pm

Georges G.E. Gielen, Katholieke Universiteit Leuven, Belgium

Future Trends for Wireless Communication Frontends in Nanometer CMOS

GARDENIA ROOM (Ground Floor)