FINAL PROGRAM

THE 12-th ACM GREAT LAKES SYMPOSIUM ON VLSI
April 18-20

Holiday Inn Martinique on Broadway
49 West 32nd Street
NEW YORK, NY 10001 USA

ON-SITE REGISTRATION HOURS:

Wednesday, 4/17: 7 pm to 8:30 pm
Thursday, 4/18 and Friday 4/19: 7:00 am to 8:30 am

ALL TECHNICAL SESSIONS WILL BE HELD IN BALLROOM A/B

THE TUTORIAL WILL BE HELD IN THE CHELSEA ROOM

THURSDAY APRIL 18

Welcome Address and Keynote Speech: 8:30 a.m. to 9:45 a.m.

8:30 a.m. to 8:45 a.m. Welcome Address

8:45 a.m. to 9:45 a.m. Keynote Address:

A VLSI System Perspective for Microprocessors Beyond 100 nm

Dr. Shekhar Borkar, Director, Intel Circuits Research Lab

Abstract: Microprocessor performance increased by five orders of magnitude in the last three decades. This was made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue to fulfill the microprocessor performance demand; however, with some adverse effects posing barriers. Therefore, performance at any cost will not be an option; significant improvements in efficiency of transistor utilization will be necessary. This paper will discuss potential solutions in all disciplines, such as microarchitecture, circuits, design technologies & methodologies, thermals, and power delivery to overcome these barriers in technologies beyond 100nm.

Key: F = Full Paper, S = Short Paper

SESSION 1. Low Power Design: 10:15 a.m. to 11:45 a.m.

Chair: Mircea Stan, Univ. of Virginia

(F) **Power and CAD Considerations for the 1.75MByte, 1.2Ghz L2 Cache of the Alpha 21364 Microprocessor**

Joel Grodstein, Rachied Rayess and Tad Truex

(F) **Multi-voltage Low Power Convolvers Using the Polynomial Residue Number System**
V. Paliouras, A. Skavantzos and T. Stouraitis

(F) **Properties of On-chip Inductive Current Loops**
Andrey V. Mezhiba and Eby G. Friedman

(S) **Enhanced Clustered Voltage Scaling for Low Power**
Monica Donno, Luca Macchiarulo, Alberto Macii, Enrico Macii and Massimo Poncino

SESSION 2. Energy and Delay Considerations: 1 p.m. to 2:45 p.m.

Chair: Alberto Macii, Polytecnico di Torino

(F) **Unified Architecture Level Energy-Efficiency Metric**
Victor Zyuban

(F) **Fast and Accurate Wire Delay Estimation for Physical Synthesis of Large ASICs**
Ruchir Puri, David S. Kung and Anthony D. Drumm

(F) **A Compact Delay Model for Series-Connected MOSFETs**
Kaveh Shakeri and James D. Meindl

(S) **A Decoupling Method for Analysis of Coupled RLC Interconnects**
Jun Chen and Lei He

(S) **Low Swing Dual Threshold Voltage Domino Logic**
Volkan Kursun and Eby G. Friedman

SESSION 3. Testing and Fault-Tolerance: 3:15 p.m. to 5 p.m.

Chair: Zhigang (David) Pan, IBM

(F) **An Error Simulation Based Approach to Measure Error Coverage of Formal Properties**
P.Azzoni A.Fedeli F.Fummi G.Pravadelli U.Rossi and F.Toto

(F) **Protected IP-Core Test Generation**
Alessandro Fin and Franco Fummi

(F) **Test Generation for Resistive Opens in CMOS**
Arun Krishnamachary and Jacob. A. Abraham

(S) **Self-Checking Sequential Circuits with Self-Healing Ability**
Ilya Levin, Vladimir Ostrovsky, Sergey Ostanin and Mark Karpovsky

(S) **Minimizing Concurrent Test Time in SoC's by Balancing Resource Usage**
Dan Zhao and Shambhu Upadhyaya

POSTER SESSION: 5 p.m. to 6:30 p.m.

Chair: Patrick Madden, SUNY-Binghamton

FRIDAY APRIL 19

SESSION 4. VLSI Design: 8:30 a.m to 10:00 a.m.

Chair: Martin Margala, Univ. of Rochester

(F) **Efficient Implementation of a Complex +/- 1 Multiplier**
Boris D. Andreev, Eby G. Friedman, and Edward L. Titlebaum

(F) **On the High-Speed VLSI Implementation of Errors-and-Erasures Correcting Reed-Solomon Decoders**
Tong Zhang and Keshab K. Parhi

(F) **Design Limitations in Deep sub-0.1micron CMOS SRAM Circuits for High-Performance On-Chip Cache Applications**
Robert K. Grube, Wang Qi and Sung-Mo Kang

(S) **Reconfigurable Repetitive Padding Unit**
Georgi Kuzmanov and Stamatis Vassiliadis

SESSION 5. VLSI Circuits: 10:15 a.m. to 11:45 a.m.

Chair: Eby Friedman, Univ. of Rochester

(F) **Energy-Delay Efficiency of VLSI Computations**
Paul I. Penzes, Alain J. Martin

(F) **Active Shields: A New Approach to Shielding Global Wires**
Himanshu Kaul, Dennis Sylvester and David Blaauw

(F) **Variable-Segment & Variable-Driver Parallel Regeneration Techniques for RLC VLSI Interconnects**
Falah R. Awwad and Mohamed Nekili

(S) **Selective Run Built-In Self-Test Using an Embedded Processor**
Sungbae Hwang and Jacob A. Abraham

SESSION 6. Design Automation: 1 p.m. to 2:45 p.m.

Chair: Ken Shepard, Columbia Univ.

(F) **Board-Level Multiterminal Net Assignment**
Xiaoyu Song, William N. N. Hung, Alan Mishchenko, Malgorzata, Chrzanowska-Jeske, Alan Coppola and Andrew Kennings

(F) **Minimizing Resources in a Repeating Schedule for a Split-Node Data-Flow Graph**
Timothy W. O'Neil and Edwin H.-M. Sha

(F) **A New Look at Hardware Maze Routing**
John A. Nestor

(S) **Novel Interconnect Modeling by Using High-Order Compact Finite Difference Methods**
Qinwei Xu and Pinaki Mazumder

(S) **AQUASUN: Adaptive Window Query Processing in CAD Applications for Physical Design and Verification**
Michiel De Wilde, Dirk Stroobandt and Peter Verplaetse

SESSION 7. Potpourri: 3:15 p.m. to 4:25 p.m.

Chair: Igor Markov, Univ. of Michigan

(F) **Term Ordering Problem on MDG**
Yi Feng and Eduard Cerny

(S) **A Low Power Direct Digital Frequency Synthesizer**
Pierre Langlois and Dhamin Al-Khalili

(S) **Novel Design and Verification of a 16 x 16-b Self-Repairable Reconfigurable Inner Product Processor**
Rong Lin and Martin Margala

(S) **Computing Walsh, Arithmetic and Reed-Muller Spectral Decision Diagrams Using Graph Transformations**
W. J. Townsend, M. A. Thornton, D. M. Miller and R. Drechsler

SATURDAY APRIL 20

TUTORIAL. 8:30 a.m. to 1:30 p.m., Chelsea Room

Impact of Process Variation and Leakage on Future High Performance CMOS Circuits
by Dr. Siva Narendra and Dr. Ali Keshavarzi, Circuit Research, Intel Labs

Abstract:

In future CMOS technology generations, supply and threshold voltages will have to continually scale to sustain performance increase, limit energy consumption, control power dissipation, and maintain reliability. These continual scaling requirements on supply and threshold voltages pose several technology, circuit design, and testing challenges. As technology scales control of process variation and leakage become critical for design and testing of integrated circuits. This tutorial will cover circuit design techniques to address die-to-die, within-die, and neighborhood threshold voltage variations. Testing techniques for intrinsically leaky CMOS ICs will be explained. Topics covered include, scaling of MOS devices, predictable models and design, leakage current in CMOS circuits, leakage control techniques, adaptive body bias, low voltage analog circuits, and testing of future CMOS circuits under elevated background leakage.

Biographies:

Siva Narendra is a staff engineer at Intel Labs. He has been with Intel Labs for the past 5 years where his research focuses on low voltage analog and digital circuits. He received his Ph.D. in Electrical Engineering and Computer Science from MIT in 2002. He has numerous reviewed publications, 11 issued patents, and 31 patents pending. He is an associate editor for the IEEE Transactions on VLSI Systems, member of the 2002 ISLPED technical program committee and an adjunct faculty at the department of ECE at Oregon State University.

Ali Keshavarzi received his Ph.D. degree in electrical engineering from Purdue University, West Lafayette, Indiana. He is a staff engineer and senior researcher at Microprocessor Research Laboratories (MRL) of Intel Corporation, Portland, Oregon. He is currently focusing on long-term research in low-power/high-performance circuit techniques and device structures for future generations of microprocessors. Ali has been with Intel for eleven years, has many published papers and has more than 20 patents (7 issued and the rest are pending patents). Ali has received the best paper award at 1997 IEEE International Test Conference at Washington, D.C. on testing solutions of intrinsically leaky integrated circuits.