Session 1: Emerging Technologies and Paradigms for Low Power Computing

1) Design of a Low-Power Non-Volatile Programmable Inverter Cell for COGRE-based Circuits
Fabrizio Lombardi, Pilin Junsangsri, Salin Junsangsri and Martin Margala

2) VaLHALLA: Variable Latency History Aware Local-carry Lazy Adder
Ali Murat Gok and Nikos Hardavellas

3) Energy Efficient Magnetic Tunnel Junction Based Hybrid LSI Using Multi-Threshold UTBB-FD-SOI Device
Hao Cai, You Wang, Lirida Naviner, Wang Kang and Weisheng Zhao

4) A Mixed-Size Monolithic 3D Placer with 2D Layout Inheritance
Xu He, Yao Wang, Yang Guo and Sorin Cotofana

5) LightNN: Filling the Gap between Conventional Deep Neural Networks and Binarized Networks (Best Paper Candidate)
Ruizhou Ding, Zeye Liu, Rongye Shi, Diana Marculescu and Shawn Blanton

Session 2: Design Techniques for Non-Traditional Computing

1) Design of a Flash-based Circuit for Multi-valued Logic
Monther Abusultan and Sunil Khatri

2) Design of Approximate Logarithmic Multipliers
Weiqiang Liu, Jiahua Xu, Danye Wang and Fabrizio Lombardi

3) Mitigating the Effect of the Reliability Soft-errors of the RRAM Devices on the Performance of the RRAM-based Neuromorphic Systems
Amr Tosson, Shimeng Yu, Mohab Anis and Lan Wei

4) A Spin Transfer Torque based Cellular Neural Network (CNN) Architecture
Yu Bai

5) Neuro-NoC: Neural Network based Predictive Routing for Network-on-Chip Architectures
Michel Kinsy and Shreeya Khadka

Session 3: Strategies for In-Memory Computing

1) A Domain-Specific Language and Compiler for Computation-in-Memory Skeletons (Best Paper Candidate)
Jintao Yu, Tom Hogervorst and Razvan Nane

2) Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices
Shaahin Angizi, Zhezhi He and Deliang Fan

3) Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption
Zhezhi He, Shaahin Angizi, Farhana Parveen and Deliang Fan

4) Evaluating Data Resilience in CNNs from an Approximate Memory Perspective
Yuanchang Chen, Yizhe Zhu, Fei Qiao, Jie Han, Yuansheng Liu and Huazhong Yang

Session 4: Circuits, Architectures, and System Level Issues for Many-Core Processors

1) A Robust C-element Design with Enhanced Metastability Performance (Best Paper Candidate)
Kinshuk Sharma and Sunil Khatri

2) Circuit Level Design of a Hardware Hash Unit for use in Modern Microprocessors
Abbas Fairouz, Monther Abusultan and Sunil Khatri

3) DELCA: DVFS Efficient Low Cost Multicore Architecture
Shoumik Maiti and Sudeep Pasricha

4) EEAL: Processors' Performance Enhancement Through Early Execution of Aliased Loads
Abhishek Rajgadia, Newton Singh and Virendra Singh

5) Performance-aware resource management of multi-threaded applications on many-core systems
Daniel Olsen and Iraklis Anagnostopoulos

Session 5: CAD for the Nano Era

1) Under-the-cell Routing to Improve Manufacturability (Best Paper Candidate)
Àlex Vidal-Obiols, Jordi Cortadella and Jordi Petit

2) Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains
Zhufei Chu, Xifan Tang, Mathias Soeken, Ana Petkovska, Grace Zgheib, Luca Amaru, Yinshui Xia, Paolo Ienne, Giovanni De Micheli and Pierre-Emmanuel Gaillardon

3) Redundant Via Insertion with Cut Optimization for Self-Aligned Double Patterning
Youngsoo Song, Jinwook Jung and Youngsoo Shin

4) Boolean Decomposition for AIG optimization
Lucas Machado and Jordi Cortadella

5) Mixed-Cell-Height Standard Cell Placement Legalization
Chung-Yao Hung, Peng-Yi Chou and Wai-Kei Mak

Session 6: Hardware Security: New Advances in Timing Side Channel and Logic Obfuscation

1) Covert Timing Channels Exploiting Non-Uniform Memory Access based Architectures
Fan Yao, Guru Venkataramani and Milos Doroslovacki

2) A Low-Cost Secure GPS Spoofing Detector Design for the Internet of Things Applications (Best Paper Candidate)
Md Tanvir Arafin, Dhananjay Anand and Gang Qu

3) A Novel Side-channel Timing Attack on GPUs
Zhen Hang Jiang, Yunsi Fei and David Kaeli

4) Cyclic Obfuscation for Creating SAT-Unresolvable Circuits
Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan and Yier Jin

5) Double DIP: Re-Evaluating Security of Logic Encryption Algorithms
Yuanqi Shen and Hai Zhou

Session 7: Testing and Reliability

1) Efficient Critical Path Selection Under a Probabilistic Delay Model (Best Paper Candidate)
Ahish Mysore Somashekar and Spyros Tragoudas

2) Combining Restorability and Error Detection Ability for Effective Trace Signal Selection
Binod Kumar, Ankit Jindal, Masahiro Fujita and Virendra Singh

3) Radiation-Hardened Designs for Soft-Error-Rate Reduction by Delay-Adjustable D-Flip-Flops
Yuwen Lin, Charles H.-P. Wen and Herming Chiueh

4) Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs
Luca Sterpone, Sarah Azimi, Boyang Du, David Merodio Codinachs and Raoul Grimoldi

5) Energy Efficient Adaptive Approach for Dependable Performance in the presence of Timing Interference
Nikolaos Zompakis, Michail Noltsis, Dimitrios Rodopoulos, Francky Catthoor and Dimitrios Soudris

Session 8: Emerging Technologies, RF Circuits and Security Functions

1) Design Automation for Paper Microfluidics with Passive Flow Substrates
Joshua Potter, William Grover and Philip Brisk

2) Neuromorphic 3D Integrated Circuit: A Hybrid, Reliable and Energy Efficient Approach for Next Generation Computing (Best Paper Candidate)
Md Amimul Ehsan, Zhen Zhou and Yang Yi

3) Method for Phase Noise Analysis of RF Circuits
Dimo Martev, Sven Hampel and Ulf Schlichtmann

4) Revealing On-chip Proprietary Security Functions with Scan Side Channel Based Reverse Engineering
Leonid Azriel, Ran Ginosar and Avi Mendelson

Session 9: CAD under Challenges: Tight Constraints and Unreliability

1) Analysis of Single Event Upsets in Combinational Designs at RTL Based on Satisfiability Modulo Theories
Ghaith Kazma, Ghaith Bany Hamad, Otmane Ait Mohamed and Yvon Savaria

2) Fine-Grain Program Snippets Generator for Mobile Core Design
Shuang Song, Raj Desikan, Mohamad Barakat, Sridhar Sundaram, Andreas Gerstlauer and Lizy K. John

3) Coupling-Aware Functional Timing Analysis for Tighter Bounds: How Much Margin Can We Relax?
Jack S.-Y. Lin, Louis Y.-Z. Lin, Ryan H.-M. Huang and Charles H.-P. Wen

4) Thermal Constrained Energy Efficient Real-Time Scheduling on Multi-Core Platforms
Shi Sha, Wujie Wen, Shaolei Ren and Gang Quan

5) Quantitative Modeling of Thermo-Optic Effects in Optical Networks-on-Chip
Weichen Liu, Peng Wang, Mengquan Li, Yiyuan Xie and Nan Guan

Session 10: Memory Design from Circuits to Architectures

1) A Reconfigurable Replica Bitline to Determine Optimum SRAM Sense Amplifier Set Time
Samira Ataei and James Stine

2) Building a Fast and Power Efficient Inductive Charge Pump System for 3D Stacked Phase Change Memories

Lei Jiang, Sparsh Mittal and Wujie Wen

3) Design Space Exploration of TAGE Branch Predictor with Ultra-Small RAM
Chaobing Zhou, Libo Huang, Zhisheng Li, Tan Zhang and Qiang Dou

4) A Power Efficient Architecture with Optimized Parallel Memory Accessing for Feature Generation
Peng Ouyang, Shouyi Yin, Chunxiao Xing, Leibo Liu and Shaojun Wei

5) Design of Approximate High-Radix Dividers by Inexact Binary Signed-Digit Addition
Fabrizio Lombardi, Linbin Chen, Weiqiang Liu, Jie Han and Paolo Montuschi