GLSVLSI Welcome Remarks:
9:00am – 9:10am, Wednesday, May 10, 2017
MT Temple A

Keynote 1
9:15am – 10:00 am, Wednesday, May 10, 2017
MT Temple A

Moderator: Deming Chen, University of Illinois at Urbana-Champaign, USA
Cognitive Data-centric Systems,
Leland Chang, Senior manager VLSI Design, IBM Research

Session 1: Emerging Technologies and Paradigms for Low Power Computing
10:20am-12:00pm, Wednesday, May 10, 2017
Lakeshore

Session Chairs
Deliang Fan, University of Central Florida, USA (Chair)
Deming Chen, University of Illinois at Urbana-Champaign, USA (Co-Chair)

1) Design of a Low-Power Non-Volatile Programmable Inverter Cell for COGRE-based Circuits
Fabrizio Lombardi, Pilin Junsangsri, Salin Junsangsri and Martin Margala

2) VaLHALLA: Variable Latency History Aware Local-carry Lazy Adder
Ali Murat Gok and Nikos Hardavellas

3) Energy Efficient Magnetic Tunnel Junction Based Hybrid LSI Using Multi-Threshold UTBB-FD-SOI Device
Hao Cai, You Wang, Lirida Naviner, Wang Kang and Weisheng Zhao

4) A Mixed-Size Monolithic 3D Placer with 2D Layout Inheritance
Xu He, Yao Wang, Yang Guo and Sorin Cotofana

5) LightNN: Filling the Gap between Conventional Deep Neural Networks and Binarized Networks (Best Paper Candidate)
Ruizhou Ding, Zeye Liu, Rongye Shi, Diana Marculescu and Shawn Blanton

Session 2: Design Techniques for Non-Traditional Computing
10:20am-12:00pm, Wednesday, May 10, 2017
Beehive

Session Chairs
Wujie Wen, Florida International University, USA (Chair)
Gang Qu, University of Maryland, USA (Co-Chair)

1) Design of a Flash-based Circuit for Multi-valued Logic
Monther Abusultan and Sunil Khatri

2) Design of Approximate Logarithmic Multipliers
Weiqiang Liu, Jiahua Xu, Danye Wang and Fabrizio Lombardi

3) Mitigating the Effect of the Reliability Soft-errors of the RRAM Devices on the Performance of the RRAM-based Neuromorphic Systems
Amr Tosson, Shimeng Yu, Mohab Anis and Lan Wei

4) A Spin Transfer Torque based Cellular Neural Network (CNN) Architecture
Yu Bai

5) Neuro-NoC: Neural Network based Predictive Routing for Network-on-Chip Architectures
Michel Kinsy and Shreeya Khadka

Session 3: Strategies for In-Memory Computing
1:30pm-2:50pm, Wednesday, May 10, 2017
Lakeshore

Session Chairs
Weisheng Zhao, Beihang University, China (Chair)
Miroslav Velev, Aries Design Automation, USA (Co-Chair)

1) A Domain-Specific Language and Compiler for Computation-in-Memory Skeletons (Best Paper Candidate)
Jintao Yu, Tom Hogervorst and Razvan Nane

2) Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices
Shaahin Angizi, Zhezhi He and Deliang Fan

3) Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption
Zhezhi He, Shaahin Angizi, Farhana Parveen and Deliang Fan

4) Evaluating Data Resilience in CNNs from an Approximate Memory Perspective
Yuanchang Chen, Yizhe Zhu, Fei Qiao, Jie Han, Yuansheng Liu and Huazhong Yang

Special Session 1: Low Power Computing based on Non-Volatile Memories
1:30pm-2:50pm, Wednesday, May 10, 2017
Beehive

Session Chairs
Chair: Weisheng Zhao, Beihang University

Co-chair: Damien Querlioz, University of Paris Saclay, CNRS

1) Advanced Low Power Spintronic Memories beyond STT-MRAM by Wang Kang, Zhaohao Wang, He Zhang, Sai Li, Youguang Zhang and Weisheng Zhao
2) Exploiting Non-Volatility for Information Processing by Robert Perricone, Li Tang, X. Sharon Hu and Michael Niemier
3) Neuromorphic Computing Based on Resistive RAM by Zixuan Chen, Huaqiang Wu, Bin Gao, Peng Yao, Xinyi Li and He Qian
4) Implications of the Use of Magnetic Tunnel Junctions as Synapses in Neuromorphic Systems by Adrien F. Vincent, Nicolas Locatelli, Qifan Wu and Damien Querlioz

Poster Session 1 - CAD, VLSI Design, VLSI Circuits and Power Aware Design
2:50pm – 3:50 pm, Wednesday, May 10, 2017
MT Temple A

1) A maze routing-based algorithm for ML-OARST with pre-selecting and ripping up and re-building Steiner points
Kuen-Wey Lin, Yeh-Sheng Lin, Yih-Lang Li and Rung-Bin Lin.

2) An Integrated Optimization Framework for Partitioning, Scheduling and Floorplanning on Partially Dynamically Reconfigurable FPGAs
Xiaodong Xu, Qi Xu, Jinglei Huang and Song Chen

3) Communication-aware Partitioning for Energy Optimization of Large FPGA Designs
Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan

4) Combined Centralized and Distributed Connection Allocation in Large TDM Circuit Switching NoCs
Yong Chen, Emil Matus and Gerhard Fettweis

5) Random Forest Architectures on FPGA for Multiple Applications
Xiang Lin, Shawn Blanton and Donald Thomas

6) Exploring Heterogeneous-ISA Core Architectures for High-Performance and Energy-Efficient Mobile SoCs
Wooseok Lee, Dam Sunwoo, Christopher D. Emmons, Andreas Gerstlauer and Lizy John

7) An FPGA Coarse Grained Intermediate Fabric for Regular Expression Search
Thomas Luinaud, Pierre Langlois and Yvon Savaria

8) Deadline-Aware Joint Optimization of Sleep Transistor and Supply Voltage for FinFET Based Embedded Systems
Huimei Cheng, Ji Li, Jeffrey Draper, Shahin Nazarian and Yanzhi Wang

9) Energy Savings and Performance Improvement in Subthreshold Using Adaptive Body Bias
Rajsaktish Sankaranarayanan and Matthew R. Guthaus

10) Low voltage stochastic flash ADC with front-end of inverter-based comparative unit
Xuncheng Zou, Bo Liu and Shigetoshi Nakatake

11) An Energy Combiner Design for Multiple Microbial Energy Harvesting Sources
Ridvan Umaz and Lei Wang

Session 4: Circuits, Architectures, and System Level Issues for Many-Core Processors

3:50pm-5:30pm, Wednesday, May 10, 2017
Lakeshore

Session Chairs:
Lombardi Fabrizio, Northeastern University, USA (Chair)
Ioannis Savidis, Drexel University, USA (Co-Chair)

1) A Robust C-element Design with Enhanced Metastability Performance (Best Paper Candidate)
Kinshuk Sharma and Sunil Khatri

2) Circuit Level Design of a Hardware Hash Unit for use in Modern Microprocessors
Abbas Fairouz, Monther Abusultan and Sunil Khatri

3) DELCA: DVFS Efficient Low Cost Multicore Architecture
Shoumik Maiti and Sudeep Pasricha

4) EEAL: Processors' Performance Enhancement Through Early Execution of Aliased Loads
Abhishek Rajgadia, Newton Singh and Virendra Singh

5) Performance-aware resource management of multi-threaded applications on many-core systems
Daniel Olsen and Iraklis Anagnostopoulos

Session 5: CAD for the Nano Era
3:50pm-5:30pm, Wednesday, May 10, 2017
Beehive

Session Chairs
Weichen Liu, Chongqing University, China (Chair)
Qiaoyan Yu, University of New Hampshire, USA (Co-Chair)

1) Redundant Via Insertion with Cut Optimization for Self-Aligned Double Patterning

Youngsoo Song, Jinwook Jung and Youngsoo Shin

2) Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains
Zhufei Chu, Xifan Tang, Mathias Soeken, Ana Petkovska, Grace Zgheib, Luca Amaru, Yinshui Xia, Paolo Ienne, Giovanni De Micheli and Pierre-Emmanuel Gaillardon

3) Under-the-cell Routing to Improve Manufacturability (Best Paper Candidate)
Àlex Vidal-Obiols, Jordi Cortadella and Jordi Petit

4) Boolean Decomposition for AIG optimization
Lucas Machado and Jordi Cortadella

5) Mixed-Cell-Height Standard Cell Placement Legalization
Chung-Yao Hung, Peng-Yi Chou and Wai-Kei Mak

MSE Welcome Remarks:
9:00am – 9:10am, Thursday, May 11, 2017
MT Temple A

Keynote 2
9:15am – 10:00 am, Thursday, May 11, 2017
MT Temple A
Moderator: Jie Han, University of Alberta, Canada
Internet of Medical Things,
Niraj K. Jha, Professor, Department of Electrical Engineering, Princeton University

Session 6: Hardware Security: New Advances in Timing Side Channel and Logic Obfuscation
10:20am-12:00pm, Thursday, May 11, 2017
Lakeshore

Session Chairs
Houman Homayoun, George Mason University, USA (Chair)
Guru Venkataramani, George Washington University, USA (Co-Chair)

1) Covert Timing Channels Exploiting Non-Uniform Memory Access based Architectures
Fan Yao, Guru Venkataramani and Milos Doroslovacki

2) A Novel Side-channel Timing Attack on GPUs
Zhen Hang Jiang, Yunsi Fei and David Kaeli

3) A Low-Cost Secure GPS Spoofing Detector Design for the Internet of Things Applications (Best Paper Candidate)
Md Tanvir Arafin, Dhananjay Anand and Gang Qu

4) Cyclic Obfuscation for Creating SAT-Unresolvable Circuits
Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan and Yier Jin

5) Double DIP: Re-Evaluating Security of Logic Encryption Algorithms
Yuanqi Shen and Hai Zhou

Session 7: Testing and Reliability
10:20am-12:00pm, Thursday, May 11, 2017
Beehive

Session Chairs
Chih-Tsun Huang, National Tsing Hua University, Taiwan (Chair)
Hung-Pin (Charles) Wen, National Chiao Tung University, Taiwan (Co-Chair)

1) Efficient Critical Path Selection Under a Probabilistic Delay Model (Best Paper Candidate)
Ahish Mysore Somashekar and Spyros Tragoudas

2) Combining Restorability and Error Detection Ability for Effective Trace Signal Selection
Binod Kumar, Ankit Jindal, Masahiro Fujita and Virendra Singh

3) Radiation-Hardened Designs for Soft-Error-Rate Reduction by Delay-Adjustable D-Flip-Flops
Yuwen Lin, Charles H.-P. Wen and Herming Chiueh

4) Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs
Luca Sterpone, Sarah Azimi, Boyang Du, David Merodio Codinachs and Raoul Grimoldi

5) Energy Efficient Adaptive Approach for Dependable Performance in the presence of Timing Interference
Nikolaos Zompakis, Michail Noltsis, Dimitrios Rodopoulos, Francky Catthoor and Dimitrios Soudris

Keynote 3
12:20pm – 1:20 pm, Thursday, May 11, 2017
MT Temple A
Moderator: Miroslav Velev, Aries Design Automation

FPGAs in Datacenter – Combining the Worlds of Hardware and Software Development,
Andrew Putnam, Microsoft Research Technologies (MSR-T) lab

Session 8: Emerging Technologies, RF Circuits and Security Functions
1:30pm-2:50pm, Thursday, May 11, 2017
Lakeshore

Session Chairs
Tsung-Yi Ho, National Tsing Hua University, Taiwan (Chair)
Deliang Fan, University of Central Florida, USA (Co-Chair)

1) Design Automation for Paper Microfluidics with Passive Flow Substrates
Joshua Potter, William Grover and Philip Brisk

2) Neuromorphic 3D Integrated Circuit: A Hybrid, Reliable and Energy Efficient Approach for Next Generation Computing (Best Paper Candidate)
Md Amimul Ehsan, Zhen Zhou and Yang Yi

3) Method for Phase Noise Analysis of RF Circuits
Dimo Martev, Sven Hampel and Ulf Schlichtmann

4) Revealing On-chip Proprietary Security Functions with Scan Side Channel Based Reverse Engineering

Leonid Azriel, Ran Ginosar and Avi Mendelson

Special Session 2: Three-Dimensional Integrated Circuit (3D-IC) Security
1:30pm-2:50pm, Thursday, May 11, 2017
Beehive

Session Chairs
Chair: Qiaoyan Yu, University of New Hampshire

1) Security Threats and Countermeasures in Three-Dimensional Integrated Circuits
   Jaya Dofe, Peng Gu, Dylan Stow, Qiaoyan Yu, Eren Kursun and Yuan Xie
2) Impact of Power Distribution Network on Power Analysis Attacks in Three-Dimensional Integrated Circuits
   Jaya Dofe, Zhiming Zhang, Qiaoyan Yu, Chen Yan and Emre Salman
3) The Need for Declarative Properties in Digital IC Security
   Mohamed El Massad, Frank Imeson, Siddharth Garg and Mahesh Tripunitara
4) Securing Split Manufactured ICs with Wire Lifting Obfuscated Built-In Self-Authentication
   Qihang Shi, Kan Xiao, Domenic Forte and Mark Tehranipoor

Special Session 3: Logic Obfuscation for IoT Security: A New Arms Race?
3:20pm-4:40pm, Thursday, May 11, 2017
Lakeshore

Chair: Yier Jin, University of Central Florida
Co-chair: Gang Qu, University of Maryland

1) An Empirical Study on Gate Camouflaging Methods Against Circuit Partition Attack
   Xueyan Wang, Qiang Zhou, Yici Cai and Gang Qu
2) What to Lock? Functional and Parametric Locking by Muhammad Yasin, Abhrajit Sengupta, Benjamin Carrion Schafer, Yiorgos Makris, Ozgur Sinanoglu and Jeyavijayan Rajendran
3) Circuit Obfuscation and Oracle-guided Attacks: Who Can Prevail?
   Kaveh Shamsi*, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin
4) Comparative Analysis of Hardware Obfuscation for IP Protection ,
   Sarah Amir, Bicky Shakya, Domenic Forte, Mark Tehranipoor, and Swarup Bhunia,

Industry Academia Workshop
3:20pm-4:40pm, Thursday, May 11, 2017
Beehive

Chair: Laleh Behjat, University of Calgary, Canada
Co-chair: Tina Hudson, Rose-Hulman University, USA

Keynote 4
9:00am – 10:00 am, Friday, May 12, 2017
MT Temple A
Moderator: Laleh Behjat, University of Calgary, Canada
Green Computing: New Challenges and Opportunities,
Alex Jones, Professor, University of Pittsburgh

Session 9: CAD under Challenges: Tight Constraints and Unreliability
10:20am-12:00pm, Friday, May 12, 2017
Lakeshore

Session Chairs
Jing-Jia Liou, National Tsing Hua University, Taiwan (Chair)
Wujie Wen, Florida International University, USA (Co-Chair)

1) Analysis of Single Event Upsets in Combinational Designs at RTL Based on Satisfiability Modulo Theories
Ghaith Kazma, Ghaith Bany Hamad, Otmane Ait Mohamed and Yvon Savaria

2) Fine-Grain Program Snippets Generator for Mobile Core Design
Shuang Song, Raj Desikan, Mohamad Barakat, Sridhar Sundaram, Andreas Gerstlauer and Lizy K. John

3) Coupling-Aware Functional Timing Analysis for Tighter Bounds: How Much Margin Can We Relax?
Jack S.-Y. Lin, Louis Y.-Z. Lin, Ryan H.-M. Huang and Charles H.-P. Wen

4) Thermal Constrained Energy Efficient Real-Time Scheduling on Multi-Core Platforms
Shi Sha, Wujie Wen, Shaolei Ren and Gang Quan

5) Quantitative Modeling of Thermo-Optic Effects in Optical Networks-on-Chip
Weichen Liu, Peng Wang, Mengquan Li, Yiyuan Xie and Nan Guan

Session 10: Memory Design from Circuits to Architectures
10:20am-12:00pm, Friday, May 12, 2017
Beehive

Session Chairs
Ioannis Savidis, Drexel University, USA (Chair)
Selcuk Kose, University of South Florida, USA (Co-Chair)

1) A Reconfigurable Replica Bitline to Determine Optimum SRAM Sense Amplifier Set Time
Samira Ataei and James Stine

2) Building a Fast and Power Efficient Inductive Charge Pump System for 3D Stacked Phase Change Memories
Lei Jiang, Sparsh Mittal and Wujie Wen

3) Design Space Exploration of TAGE Branch Predictor with Ultra-Small RAM
Chaobing Zhou, Libo Huang, Zhisheng Li, Tan Zhang and Qiang Dou

4) A Power Efficient Architecture with Optimized Parallel Memory Accessing for Feature Generation
Peng Ouyang, Shouyi Yin, Chunxiao Xing, Leibo Liu and Shaojun Wei

5) Design of Approximate High-Radix Dividers by Inexact Binary Signed-Digit Addition
Fabrizio Lombardi, Linbin Chen, Weiqiang Liu, Jie Han and Paolo Montuschi

Poster Session 2 - Testing/Reliability/Fault-Tolerance, Biochips and Biological Systems, Emerging Computing & Post-CMOS Technologies, Hardware Security

2:50pm – 3:50 pm, Wednesday, May 10, 2017
MT Temple A

1) Throughput Optimization for Lifetime Budgeting in Many Core Systems
Liang Wang, Xiaohang Wang, Ho-Fung Leung and Terrence Mak

2) A Test Pattern Quality Metric for Diagnosis of Multiple Stuck-at and Transition faults
Sarmad Tanwir, Michael Hsiao and Loganathan Lingappan

3) Switched Capacitor and Infinite Impulse Response Summation For A Quarter-Rate DFE With 4Gb/s Data Rate
Gyunam Jeon and Yong-Bin Kim

4) Reducing Microfluidic Very Large Scale Integration (mVLSI) Chip Area by Seam Carving
Brian Crites, Karen Kong and Philip Brisk

5) LUTOSAP: Lookup-Table-Based Online Sample Preparation in Microfluidic Biochips
Lingxuan Shao, Yibin Yang, Hailong Yao and Tsung-Yi Ho

6) ProACt: A Processor for High Performance On-demand Approximate Computing
Arun Chandrasekharan, Daniel Gro  e, and Rolf Drechsler

7) Softmax Regression Design for Stochastic Computing Based Deep Convolutional Neural Networks
Zihao Yuan, Ji Li, Zhe Li, Caiwen Ding, Ao Ren, Bo Yuan, Qinru Qiu, Jeffrey Draper and Yanzhi Wang,

8) Computing Polynomials with Positive Coefficients using Stochastic Logic by Double-NAND Expansion
Sayed Ahmad Salehi, Yin Liu, Marc Riedel and Keshab Parhi

9) On the Role of Sequential Circuits in Stochastic Computing
Pai-Shun Ting and John Hayes

10) Circuit Techniques for Online Learning of Memristive Synapses in CMOS-Memristor Neuromorphic Systems
Sagarvarma Sayyaparaju, Gangotree Chakma, Sherif Amer and Garrett S. Rose

11) Mitigating Control Flow Attacks in Embedded Systems with Novel Built-in Secure Register Bank
Sean Kramer, Zhiming Zhang, Jaya Dofe and Qiaoyan Yu

12) Using Security Invariant to Verify Confidentiality in Hardware Design
Shuyu Kong, Yuanqi Shen and Hai Zhou

13) Leveraging All-Spin Logic to Improve Hardware Security
Qutaiba Alasad, Jiann Yuan and Deliang Fan

Special Session 4: Efficient IoT Systems: The Power of Heterogenous Integration
1:30pm-2:50pm, Friday, May 12, 2017
Lakeshore

Chair: Selcuk Kose, University of South Florida
Co-chair: Ioannis Savidis, Drexel University

1) Efficient and Secure On-Chip Reconfigurable Power Delivery for IoT Devices
   Selcuk Kose
2) Design Space Modeling and Simulation for Physically Constrained 3D CPUs
   Caleb Serafy, Zhiyuan Yang and Ankur Srivastava
3) Automated Design of Stable Power Delivery Systems for Heterogeneous IoT Systems
   Inna Partin-Vaisband
4) Work Load Scheduling For Multi Core Systems With Under-Provisioned Power Delivery
   Divya Pathak, Houman Homayoun and Ioannis Savidis

Invited Session on Innovation
1:30pm-2:50pm, Friday, May 12, 2017
Beehive
Moderator: Laleh Behjat, University of Calgary, Canada
Ideation and Entrepreneurship Mindset
Dr. Alex Bruton, Professor of Entrepreneurship, University of Calgary

Innovation Exchange
3:20pm-5:30pm, Friday, May 12, 2017
MT Temple A

Chair: Tina Hudson, Rose-Hulman University, USA
Co-chair: Laleh Behjat, University of Calgary, Canada