Poster Session I

CAD, VLSI Design, VLSI Circuits and Power Aware Design

A maze routing-based algorithm for ML-OARST with pre-selecting and ripping up and re-building Steiner points
Kuen-Wey Lin, Yeh-Sheng Lin, Yih-Lang Li and Rung-Bin Lin.

An Integrated Optimization Framework for Partitioning, Scheduling and Floorplanning on Partially Dynamically Reconfigurable FPGAs
Xiaodong Xu, Qi Xu, Jinglei Huang and Song Chen

Communication-aware Partitioning for Energy Optimization of Large FPGA Designs
Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan

Combined Centralized and Distributed Connection Allocation in Large TDM Circuit Switching NoCs
Yong Chen, Emil Matus and Gerhard Fettweis

Random Forest Architectures on FPGA for Multiple Applications
Xiang Lin, Shawn Blanton and Donald Thomas

Exploring Heterogeneous-ISA Core Architectures for High-Performance and Energy-Efficient Mobile SoCs
Wooseok Lee, Dam Sunwoo, Christopher D. Emmons, Andreas Gerstlauer and Lizy John

An FPGA Coarse Grained Intermediate Fabric for Regular Expression Search
Thomas Luinaud, Pierre Langlois and Yvon Savaria

Deadline-Aware Joint Optimization of Sleep Transistor and Supply Voltage for FinFET Based Embedded Systems
Huimei Cheng, Ji Li, Jeffrey Draper, Shahin Nazarian and Yanzhi Wang

Energy Savings and Performance Improvement in Subthreshold Using Adaptive Body Bias
Rajsaktish Sankaranarayanan and Matthew R. Guthaus

Low voltage stochastic flash ADC with front-end of inverter-based comparative unit
Xuncheng Zou, Bo Liu and Shigetoshi Nakatake

Switched Capacitor and Infinite Impulse Response Summation For A Quarter-Rate DFE With 4Gb/s Data Rate
Gyunam Jeon and Yong-Bin Kim

An Energy Combiner Design for Multiple Microbial Energy Harvesting Sources
Ridvan Umaz and Lei Wang

Poster Session II

Testing/Reliability/Fault-Tolerance, Biochips and Biological Systems, Emerging Computing & Post-CMOS Technologies, Hardware Security

Throughput Optimization for Lifetime Budgeting in Many Core Systems
Liang Wang, Xiaohang Wang, Ho-Fung Leung and Terrence Mak

A Test Pattern Quality Metric for Diagnosis of Multiple Stuck-at and Transition faults
Sarmad Tanwir, Michael Hsiao and Loganathan Lingappan

Reducing Microfluidic Very Large Scale Integration (mVLSI) Chip Area by Seam Carving
Brian Crites, Karen Kong and Philip Brisk

LUTOSAP: Lookup-Table-Based Online Sample Preparation in Microfluidic Biochips
Lingxuan Shao, Yibin Yang, Hailong Yao and Tsung-Yi Ho

ProACt: A Processor for High Performance On-demand Approximate Computing
Arun Chandrasekharan, Daniel Große, and Rolf Drechsler

Softmax Regression Design for Stochastic Computing Based Deep Convolutional Neural Networks
Zihao Yuan, Ji Li, Zhe Li, Caiwen Ding, Ao Ren, Bo Yuan, Qinru Qiu, Jeffrey Draper and Yanzhi Wang,

Computing Polynomials with Positive Coefficients using Stochastic Logic by Double-NAND Expansion
Sayed Ahmad Salehi, Yin Liu, Marc Riedel and Keshab Parhi

On the Role of Sequential Circuits in Stochastic Computing
Pai-Shun Ting and John Hayes

Circuit Techniques for Online Learning of Memristive Synapses in CMOS-Memristor Neuromorphic Systems
Sagarvarma Sayyaparaju, Gangotree Chakma, Sherif Amer and Garrett S. Rose

Mitigating Control Flow Attacks in Embedded Systems with Novel Built-in Secure Register Bank
Sean Kramer, Zhiming Zhang, Jaya Dofe and Qiaoyan Yu

Using Security Invariant to Verify Confidentiality in Hardware Design
Shuyu Kong, Yuanqi Shen and Hai Zhou

Leveraging All-Spin Logic to Improve Hardware Security
Qutaiba Alasad, Jiann Yuan and Deliang Fan