The Renaissance of Analog: Enabling 6G and Beyond, AI, and Neurotechnology at the Edge

Abstract: As Moore's Law slows and the boundaries between physical and digital domains become increasingly blurred, analog design is experiencing a profound renaissance. No longer confined to niche roles, analog and mixed-signal circuits are now essential enablers of next-generation technologies, from sub-THz 6G communication systems and in-sensor AI accelerators to ultra-low-power neural interfaces and brain–computer interfaces.

This keynote will explore the evolving landscape of analog design in the post-scaling era, where energy efficiency, precision, and system-level co-design are paramount. We will examine how analog front-ends are being reimagined to support emerging paradigms such as integrated sensing and communication (ISAC), neuromorphic edge processing, and cryo-CMOS circuits for quantum computing. Special emphasis will be placed on the convergence of RF, data conversion, and bioelectronics, highlighting opportunities for analog designers to shape the future of edge intelligence.

Through recent examples and insights from advanced CMOS implementations, this talk aims to inspire the VLSI community to rethink the role of analog—not as legacy support—but as a critical, forward-driving force behind the most transformative technologies of our time.

Bio: Payam Heydari is currently the Henry Samueli Faculty Excellence Professor and the University Chancellor's Professor at the University of California, Irvine (UCI). He is the (co)-author of two books, three book chapters, and more than 200 journal and conference papers on mixed-signal, analog, radio-frequency, millimeter-wave, and terahertz integrated circuits in silicon technologies. He served as a Distinguished Lecturer of both the IEEE Solid-State Circuits Society (SSCS) (2014-2016) and the IEEE Microwave Theory and Technology Society (MTT-S) (2019-2022).

Dr. Heydari is a fellow of the National Academy of Inventors and an IEEE fellow. He was the first-place co-winner of the IEEE EMBC 2024 Young Professional Paper Competition for his work on brain-machine interfaces (BMI), and the co-recipient of the 2024 IEEE Circuits and Systems Society Darlington Best Paper Award. He received the 2023 IEEE MTT-S Distinguished Educator Award, the 2021 IEEE SSCS Innovative Education Award, and the Best Invited Paper Award at the 2021 IEEE Custom Integrated Circuits Conference (CICC). He was also the recipient of the 2016-2017 UCI School of Engineering Mid-Career Excellence in Research, the 2014 Distinguished Engineering Educator Award from Orange County Engineering Council, the 2010 Faculty of the Year Award from UCI's Engineering Student Council (ESC), the 2009 Business Plan Competition First Place Prize Award and Best Concept Paper Award both from Paul Merage School of Business at UCI, the 2009 School of Engineering Fariborz Maseeh Best Faculty

Research Award, the 2007 IEEE Circuits and Systems Society Guillemin-Cauer Award, the 2005 IEEE Circuits and Systems Society Darlington Best Paper Award, the 2005 National Science Foundation (NSF) CAREER Award, the 2005 Henry Samueli School of Engineering Teaching Excellence Award, the Best Paper Award at the 2000 IEEE Int'l Conference on Computer Design (ICCD). His research on novel low-power multi-purpose multi-antenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE Int'l Symposium on Low-Power Electronics and Design (ISLPED).

Dr. Heydari was an Associate Editor (AE) of the IEEE Journal of Solid-State Circuits (JSSC), IEEE Open Journal of Solid-State Circuits Society (OJ-SSCS), IEEE Solid-State Circuits Letters} (SSC-L) and IEEE Transactions on Circuits and Systems—I: Regular Papers (TCAS-I). He served on the Technical Program Committee (TPC) of the IEEE International Microwave Symposium (IMS), the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE European Solid-State Circuits Conference (ESSCIRC), and CICC. From 2018 to 2020, he was the AdCom member of the IEEE SSCS. He is the director of the Nanoscale Communication IC (NCIC) Labs.